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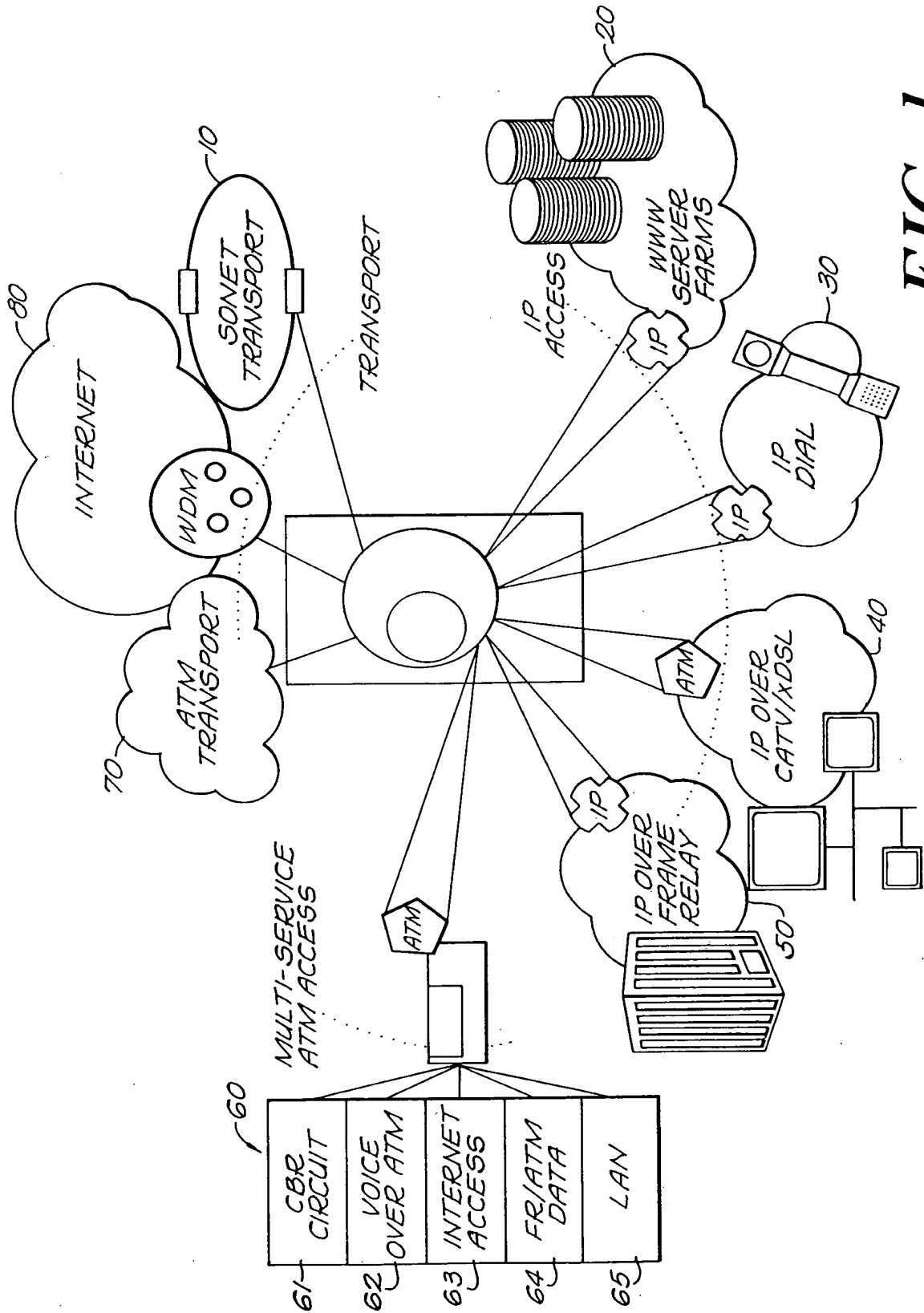


FIG. 1

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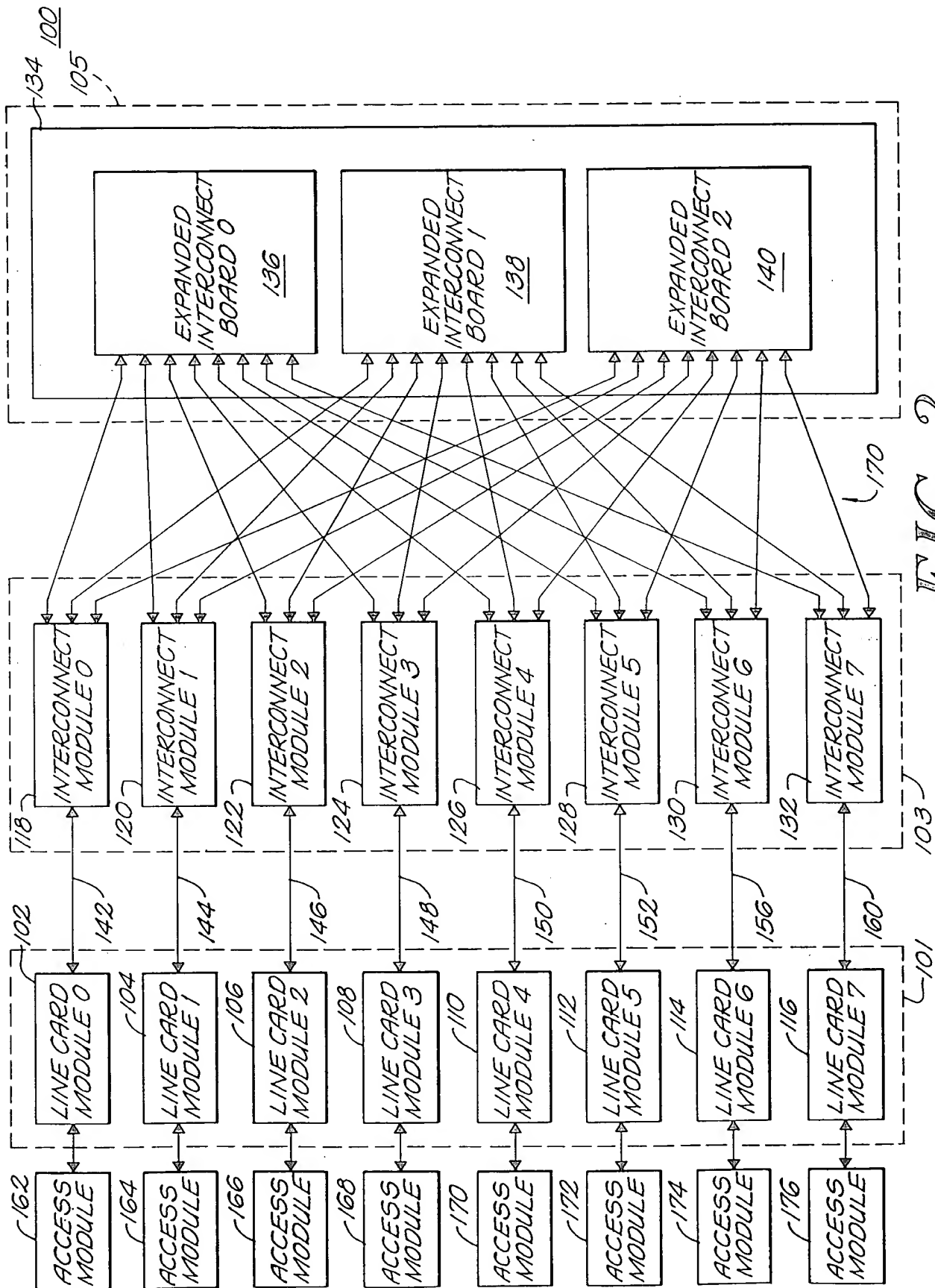


FIG. 2

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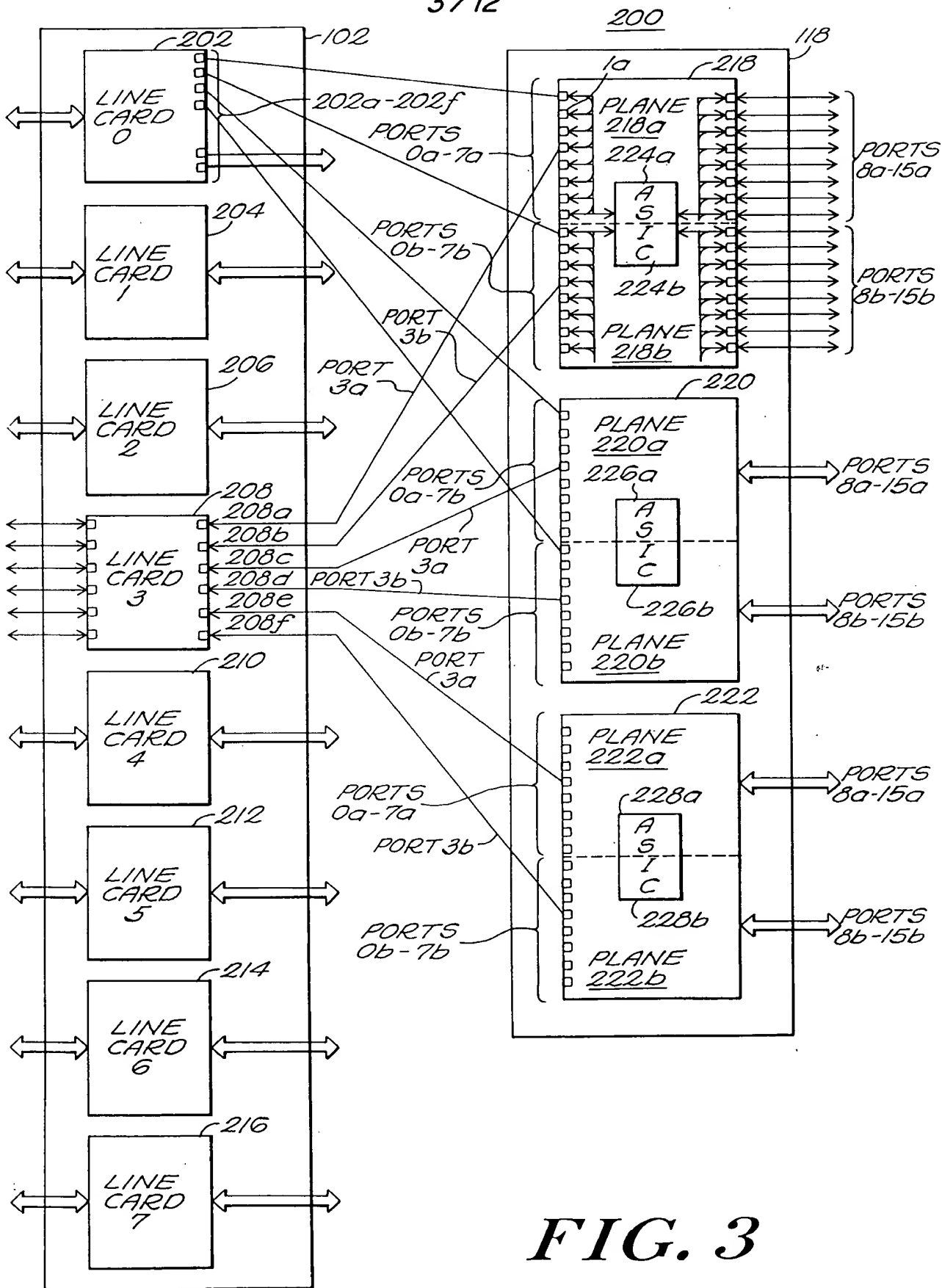


FIG. 3

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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300

302

304

<u>Source Line Card #</u>	<u>Destination Port #s (Plane, Port)</u>
202	[(218a,0a),(218b,0b),(220a,0a),(220b,0b),(222a,0a),(222b,0b)]
204	[(218a,1a),(218b,1b),(220a,1a),(220b,1b),(222a,1a),(222b,1b)]
206	[(218a,2a),(218b,2b),(220a,2a),(220b,2b),(222a,2a),(222b,2b)]
208	[(218a,3a),(218b,3b),(220a,3a),(220b,3b),(222a,3a),(222b,3b)]
210	[(218a,4a),(218b,4b),(220a,4a),(220b,4b),(222a,4a),(222b,4b)]
212	[(218a,5a),(218b,5b),(220a,5a),(220b,5b),(222a,5a),(222b,5b)]
214	[(218a,6a),(218b,6b),(220a,6a),(220b,6b),(222a,6a),(222b,6b)]
216	[(218a,7a),(218b,7b),(220a,7a),(220b,7b),(222a,7a),(222b,7b)]

FIG. 4

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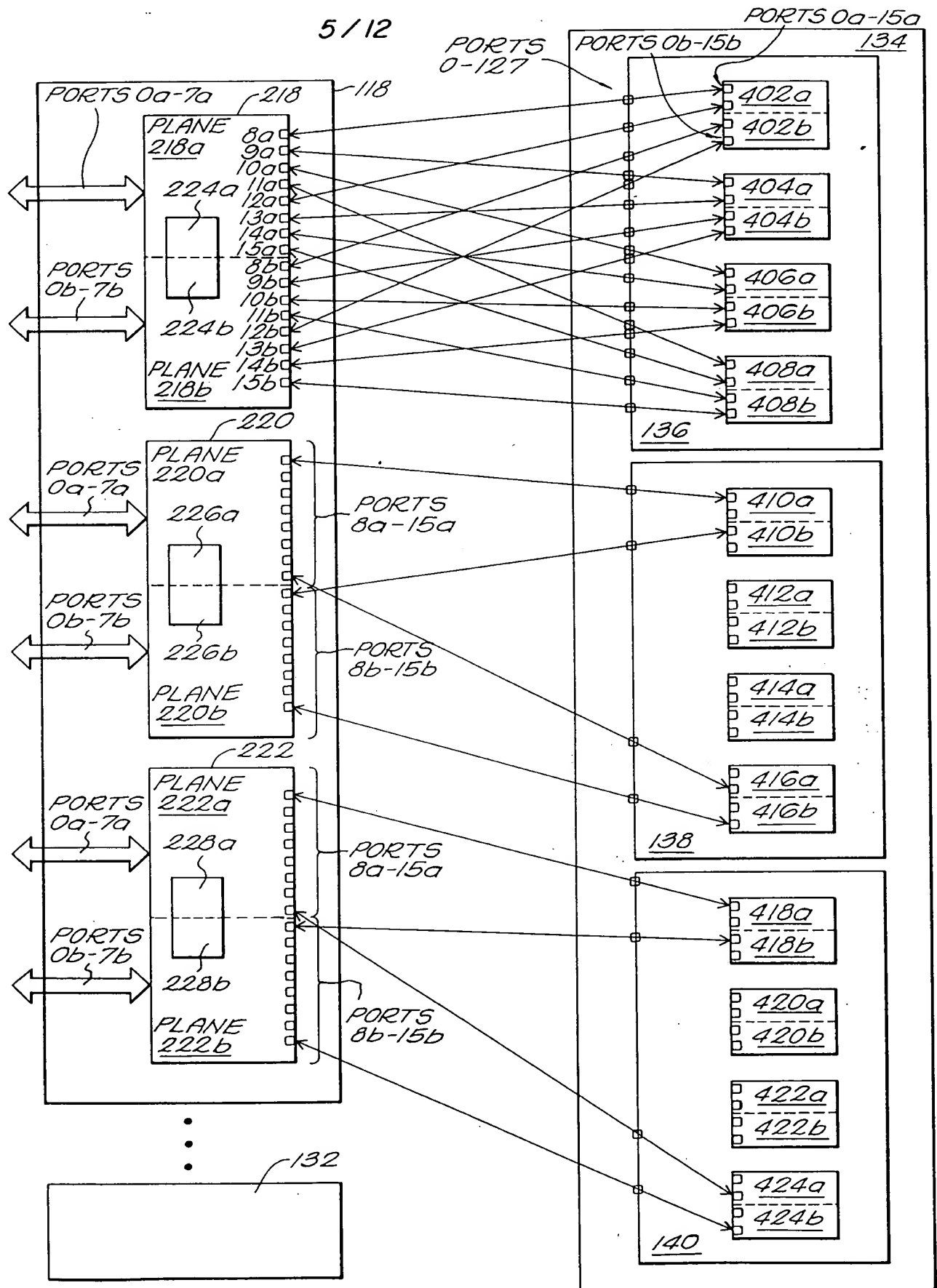


FIG. 5

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Expanded Interconnect (ASIC, Port #)			
502	504	506	508
<u>Local Interconnect</u> <u>Chassis Port #</u>	<u>For Interconnect</u> <u>Board 218</u>	<u>For Interconnect</u> <u>Board 220</u>	<u>For Interconnect</u> <u>Board 222</u>
8a	402a, 0	410a, 0	418a, 0
8b	402b, 0	410b, 0	418b, 0
9a	404a, 0	412a, 0	420a, 0
9b	404b, 0	412b, 0	420b, 0
10a	406a, 0	414a, 0	422a, 0
10b	406b, 0	414b, 0	422b, 0
11a	408a, 0	416a, 0	424a, 0
11b	408b, 0	416b, 0	424b, 0
12a	402a, 8	410a, 8	418a, 8
12b	402b, 8	410b, 8	418b, 8
13a	404a, 8	412a, 8	420a, 8
13b	404b, 8	412b, 8	420b, 8
14a	406a, 8	414a, 8	422a, 8
14b	406b, 8	414b, 8	422b, 8
15a	408a, 8	416a, 8	424a, 8
15b	408b, 8	416b, 8	424b, 8

FIG. 6

APPROVED	O.G. FIG.	
BY •	CLASS	SUBCLASS
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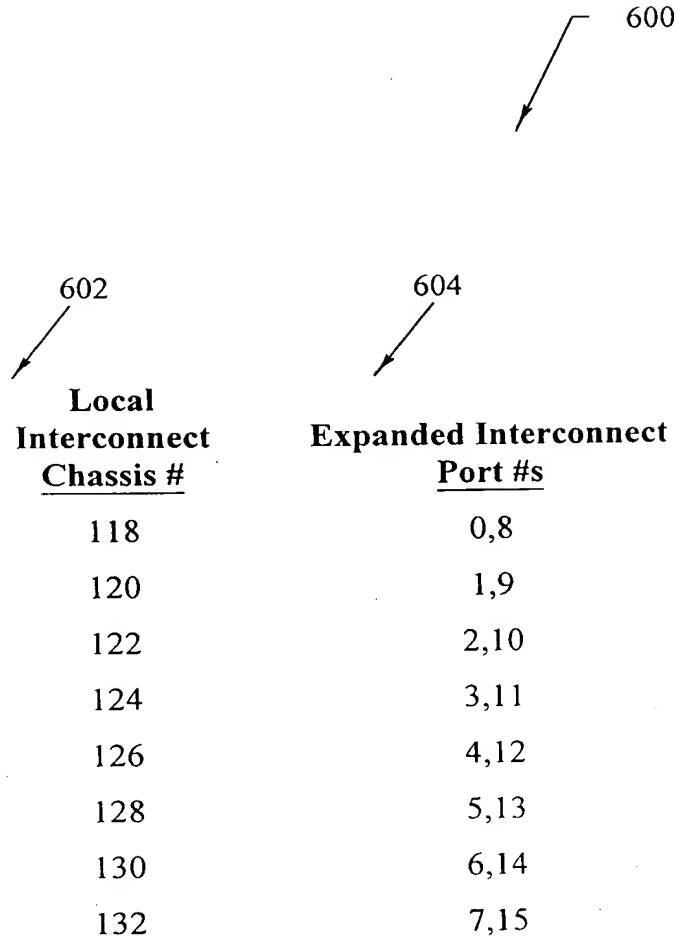


FIG. 7

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

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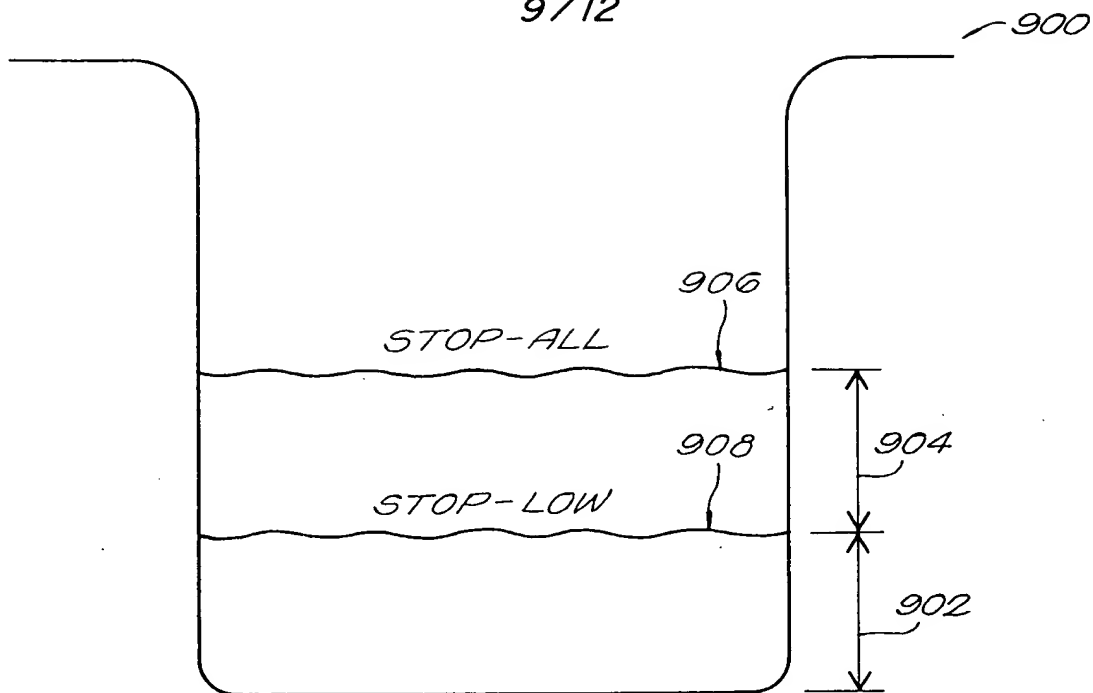


FIG. 9A

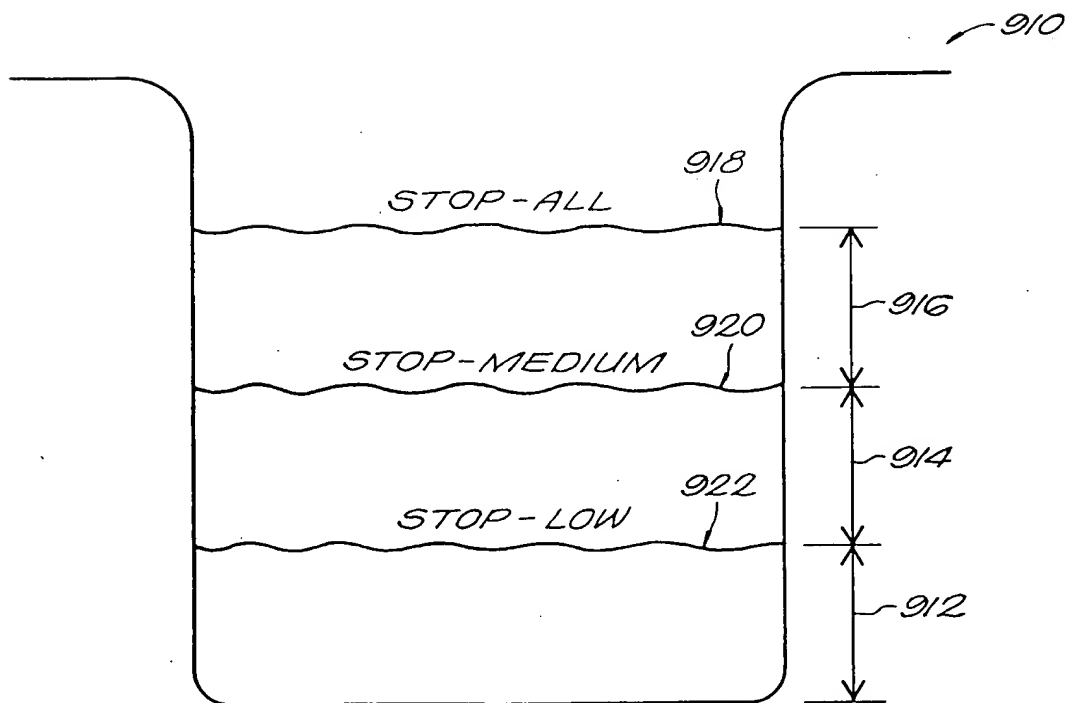


FIG. 9B

663450" 06032250

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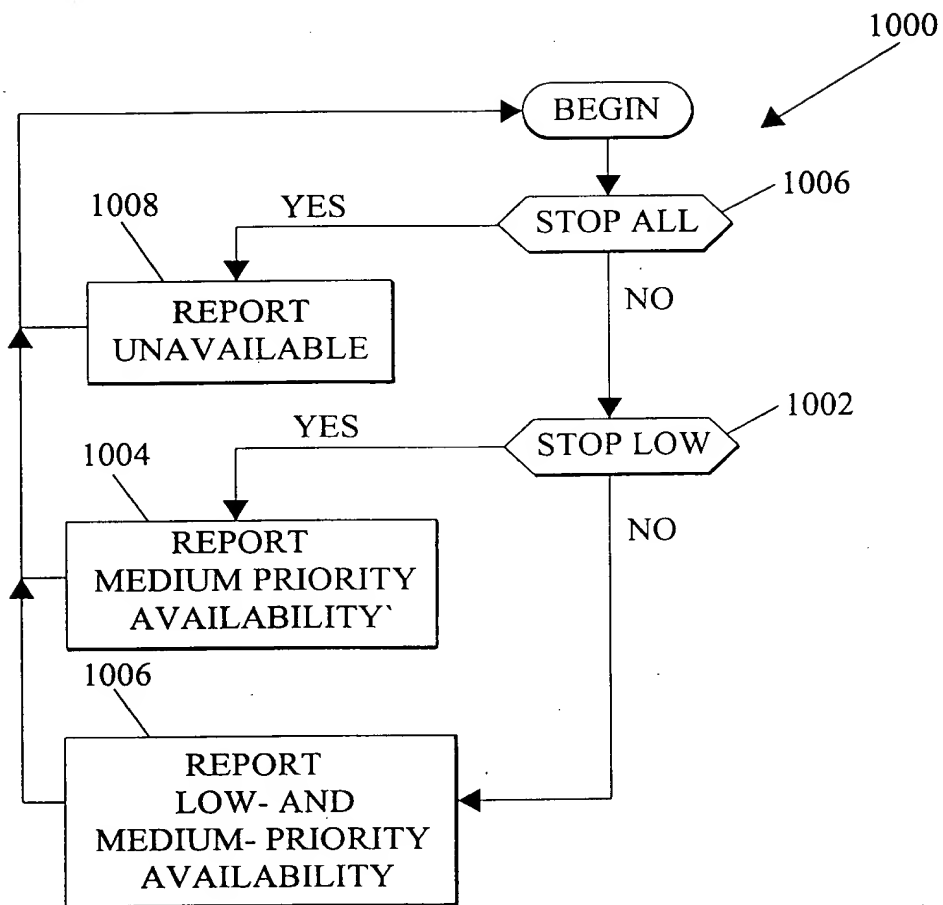


FIG. 10A

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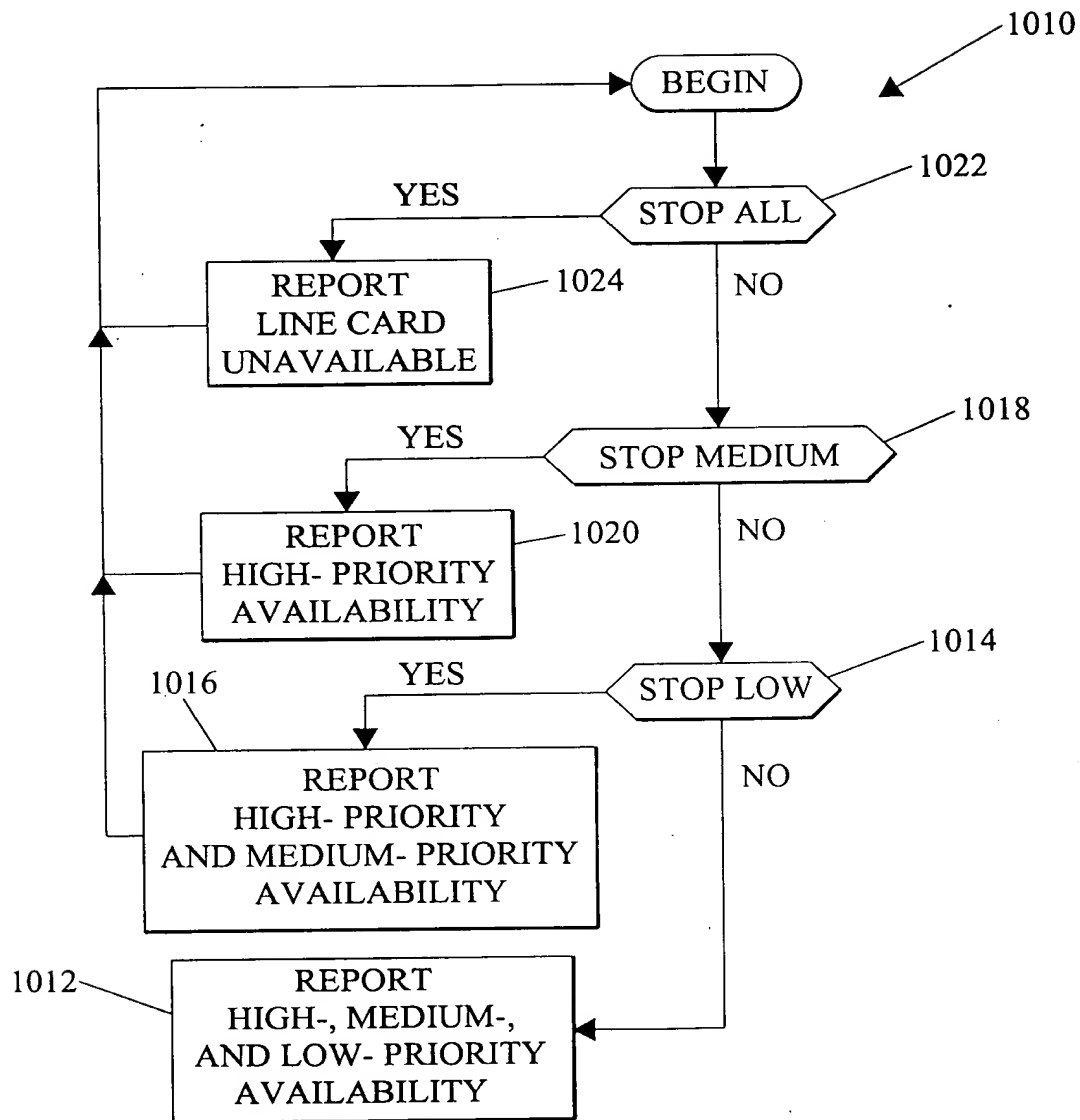


FIG. 10B

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136a

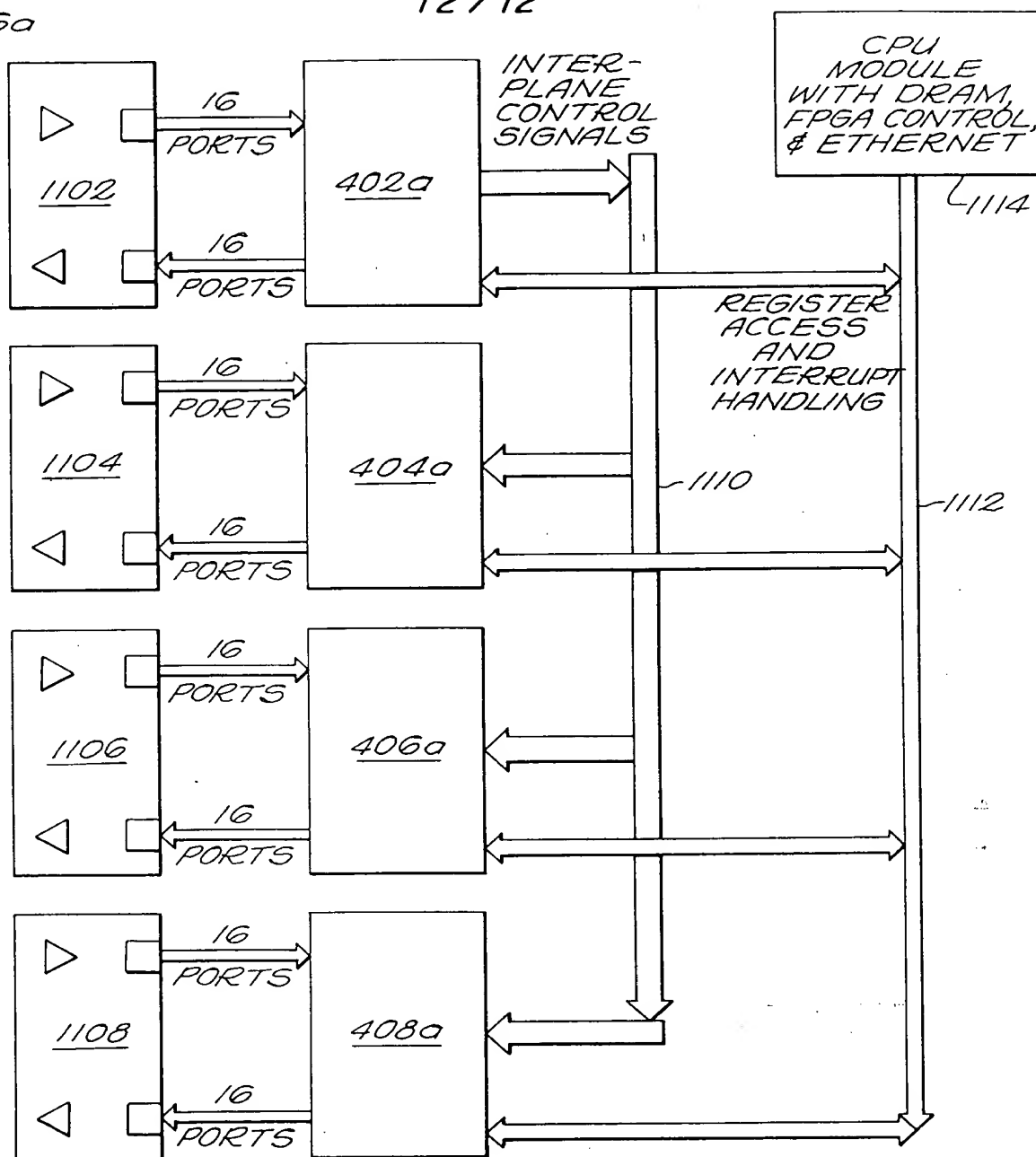


FIG. 11